Appl. No. 10/715,658
Examiner: WILSON, CHRISTIAN D, Art Unit 2891
In response to the Office Action dated March 30, 2005

Date: June 30, 2005
Attorney Docket No. 10113191

REMARKS

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority and receipt of the certified copy of the priority document. Responsive to the Office Action mailed on March 30, 2005 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1-22 are pending. Claim 21 is objected to as being a substantial duplicate of claim 10. Claims 1-5 and 9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 6,475,916) in view of Mandelman et al (US 6,674,139). Claims 6, 7, 8, and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al and Mandelman et al and further in view of Dokumaci et al (US 2004/0135212). Claims 11-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al in view of Mandelman et al and Dokumaci et al.

In this paper, claim 21 has been amended to depend from claim 11 according to the suggestion of the Examiner. Applicant submits that the objection to claim 21 is thereby overcome.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Rejections Under 103(a)

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al in view of Mandelman et al. The rejection is respectfully traversed for the reasons as follow.

Claim 1 recites a damascene gate process comprising the steps of:

providing a semiconductor substrate having a pad layer and a etch stop layer formed thereon;

forming an insulating layer to cover the etch stop layer;

forming an opening be partially removing the insulating layer, the etch stop layer, and the pad layer;

forming a protective spacer on the sidewall of the opening, wherein the tops of the protective spacer are lower than the insulating layer;

forming a gate conducting layer in the opening;

removing the protective spacer and ***the insulating layer to expose a portion of the semiconductor substrate and the etch stop layer;***

implanting the exposed semiconductor substrate to form lightly doped drains...

Thus, in claim 1, the steps for forming LDD regions comprise removing the protective spacer and the insulating layer to expose a portion of the semiconductor substrate and the etch stop layer, and implanting the exposed semiconductor substrate to form lightly doped drains. Namely, an insulating layer as well as the protective spacer are removed to expose the etch stop layer underlying the insulating layer (see line 4 of claim 1) and to expose a portion of the semiconductor substrate. The exposed semiconductor substrate is then implanted to form the LDD regions. See page 6, lines 5-14 and Figs. 1L-1N of the application.

MPEP 2142 reads in part:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In connection with the third criteria, MPEP 2143.03 goes on the state:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

The rejection of claim 1 over Lee et al in view of Mandelman et al relies on Mandelman et al for the teaching of steps of forming the LDD regions. Applicant submits that the teaching of Mandelman et al is mischaracterized in the office action.

Mandelman et al teach an inverse T-gate structure using damascene processing. Specifically, the spacers 70, 75 are removed by selective etch to expose the underlying inverse-T shape of the gate conductor 40, 80. Next, LDD implant is conducted using gate conductor 40, 80 as a mask. The implant is blocked by the thicker portions of the gate 80, but passes through the thinner portions of the gate 40. See col. 6, lines 35-43 and Fig. 7 of Mandelman et al.

Applicant respectfully submits that Mandelman et al do not teach or suggest the steps of "removing the insulating layer ... to expose a portion of the semiconductor substrate and the etch stop layer" as recited in claim 1. On the contrary, Mandelman et al merely teach removing a protective spacer 70, 75 to expose the gate conductor 40, 80. ***There is no removal of an insulating layer, and the substrate 10 and an etch stop layer are not exposed in this step.*** See Fig. 7 of Mandelman et al.

In addition, Mandelman et al also fail to teach or suggest the step of "implanting the ***exposed*** semiconductor substrate to form the LDD regions" as recited in claim 1. On the contrary, in Mandelman et al, after removal of the protective spacer 70, 75 to expose the gate conductor 40, 80, a step of implanting ***through the gate conductor 40*** is conducted to form LDD regions 90, 95 in the substrate. See Fig. 7 of Mandelman et al.

Thus, contrary to the characterization in the office action, in Mandelman et al's process for forming LDD regions, an insulating layer is not removed, a portion of a substrate and an etch stop layer are not exposed, and an implantation is not performed on an exposed substrate.

For at least the reasons described above, it is Applicant's belief that, even when taken in combination, the prior art references do not teach or suggest all the limitations of claim 1. For at least this reason, the office action fails to establish a *prima facie* case of obviousness in connection with this claim.

As it is Applicant's belief that a *prima facie* case of obviousness is not established in connection with claim 1, the Examiner's arguments in connection with the dependent claims are considered moot and are not addressed here. Withdrawal of the rejections of claims 1-10 is respectfully requested.

Rejections of claims 11-22 under 35 U.S.C. 103

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al in view of Mandelman et al and Dokumaci et al. The rejection is respectfully traversed for the reasons as follow.

Claim 11 recites a damascene gate process comprising the steps of:

providing a semiconductor substrate having a plurality of shallow trench isolation (STI) structures, an STI protective layer is formed on each of the STI structures;

sequentially forming a pad layer and an etch stop layer between the STI structures;

forming an insulating layer to cover the STI structures and the etch stop layer;

forming an opening between the structures by partially removing the insulating layer, the etch stop layer, and the pad layer;

forming a protective spacer on the sidewall of the opening, wherein the tops of the protective spacer are lower than the insulating layer;

forming dissimilar conducting layers acting as gate conducting layer in the bottom of the opening;

removing the protective spacer and ***the insulating layer to expose a portion of the semiconductor substrate and the etch stop layer;***

implanting the exposed semiconductor substrate to form lightly doped drains...

Claim 11 includes the same steps for forming the LDD regions as recited in claim 1, namely removing the protective spacer and the insulating layer to expose a portion of the semiconductor substrate and the etch stop layer, and implanting the exposed semiconductor substrate to form lightly doped drains.

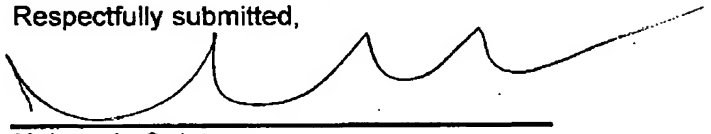
As the rejection of claim 11 also relies on Mandelman et al for the teaching of steps for forming the LDD regions, it fails to establish a *prima facie* case of obviousness for the same reasons discussed in connection with claim 1.

As it is Applicant's belief that a *prima facie* case of obviousness is not established in connection with claim 11, the Examiner's arguments in connection with the dependent claims are considered moot and are not addressed here. Withdrawal of the rejections of claims 11-22 is respectfully requested.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so.

Respectfully submitted,



Nelson A. Quintero
Reg. No. 52,143
Customer No. 34,283
Telephone: (310) 401-6180

P111364NAQ